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Sedayao et al.

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(54) **INTERRUPT BLOCKER**

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G06F 13/24	(2006.01)
H04M 3/436	(2006.01)

(52) **U.S. Cl.**

CPC ***G06F 13/24*** (2013.01); ***H04M 3/436*** (2013.01)

(58) **Field of Classification Search**

CPC H04M 3/436
USPC 379/210.02; 455/417
See application file for complete search history.

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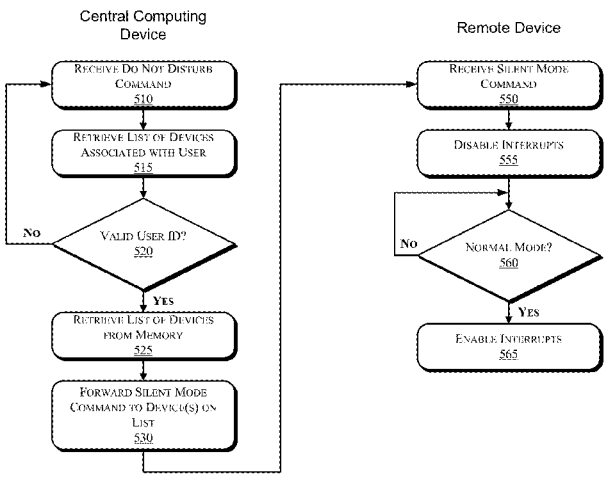
(57) **ABSTRACT**

A method comprises maintaining, in a first electronic device, a list of one or more electronic devices associated with a user, receiving, in the first electronic device, a first command, in response to the first command, forwarding a command to block interrupts on one or more electronic devices on the list of electronic devices. Other embodiments may be described.

18 Claims, 5 Drawing Sheets



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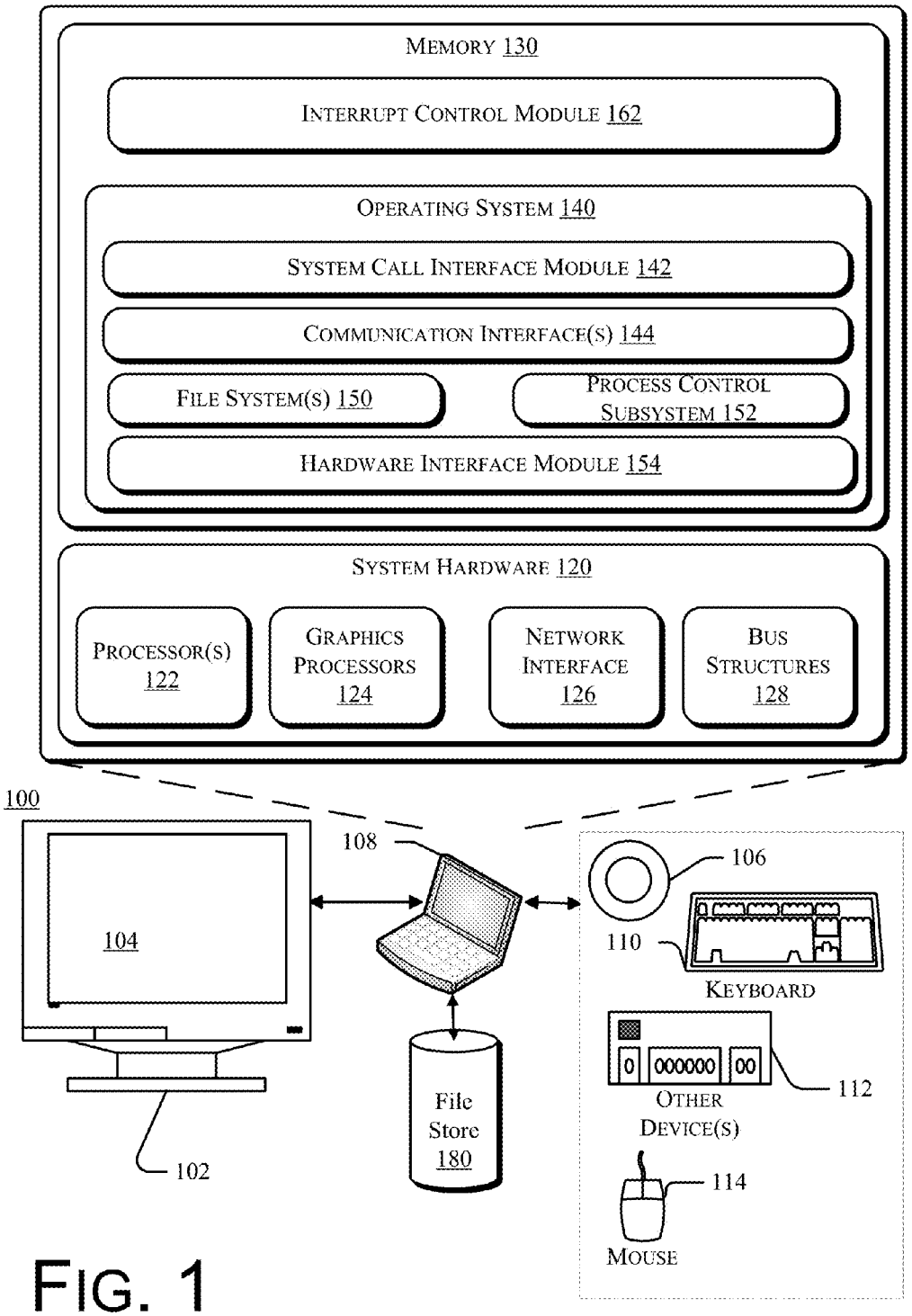
MEMORY 130
INTERRUPT CONTROL MODULE 162
OPERATING SYSTEM 140
SYSTEM CALL INTERFACE MODULE 142
COMMUNICATION INTERFACE(S) 144
FILE SYSTEM(S) 150
PROCESS CONTROL SUBSYSTEM 152
HARDWARE INTERFACE MODULE 154
SYSTEM HARDWARE 120
PROCESSOR(S) 122
GRAPHICS PROCESSORS 124
NETWORK INTERFACE 126
BUS STRUCTURES 128
100
104
102
108
File Store 180
106
110
KEYBOARD
OTHER DEVICE(S)
112
114
MOUSE

FIG. 1

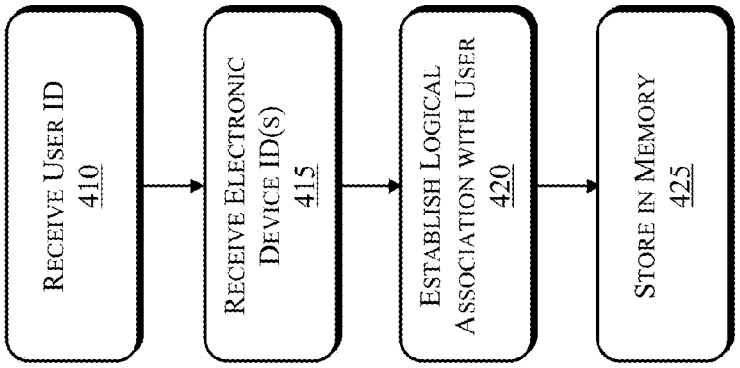
Receive User ID
410
Receive Electronic Device ID(s)
415
Establish Logical Association with User
420
Store in Memory
425

FIG. 4

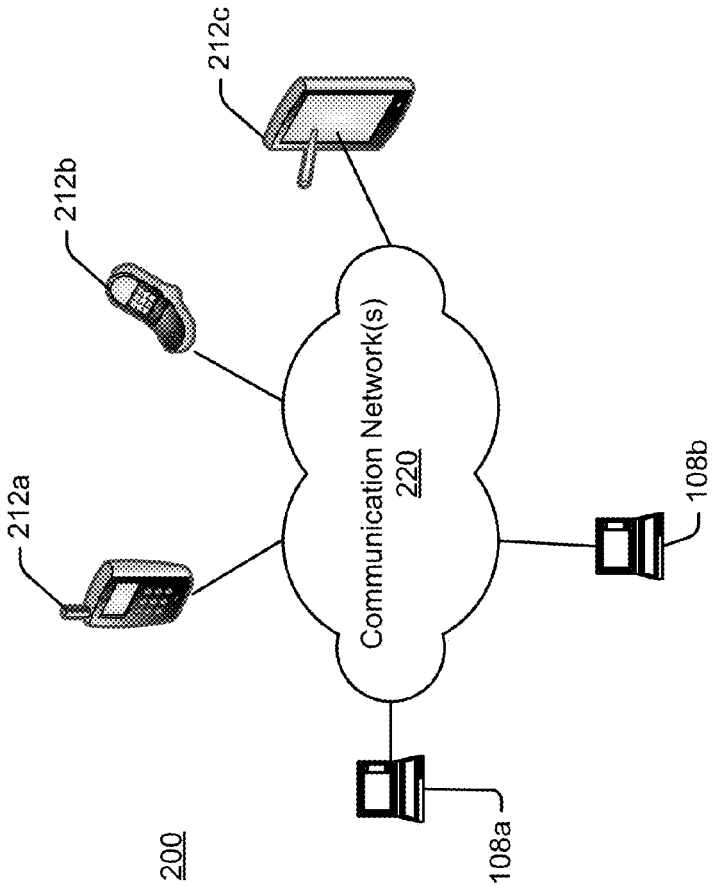
200
212a
212b
212c
Communication Network(s)
220
108a
108b

FIG. 2

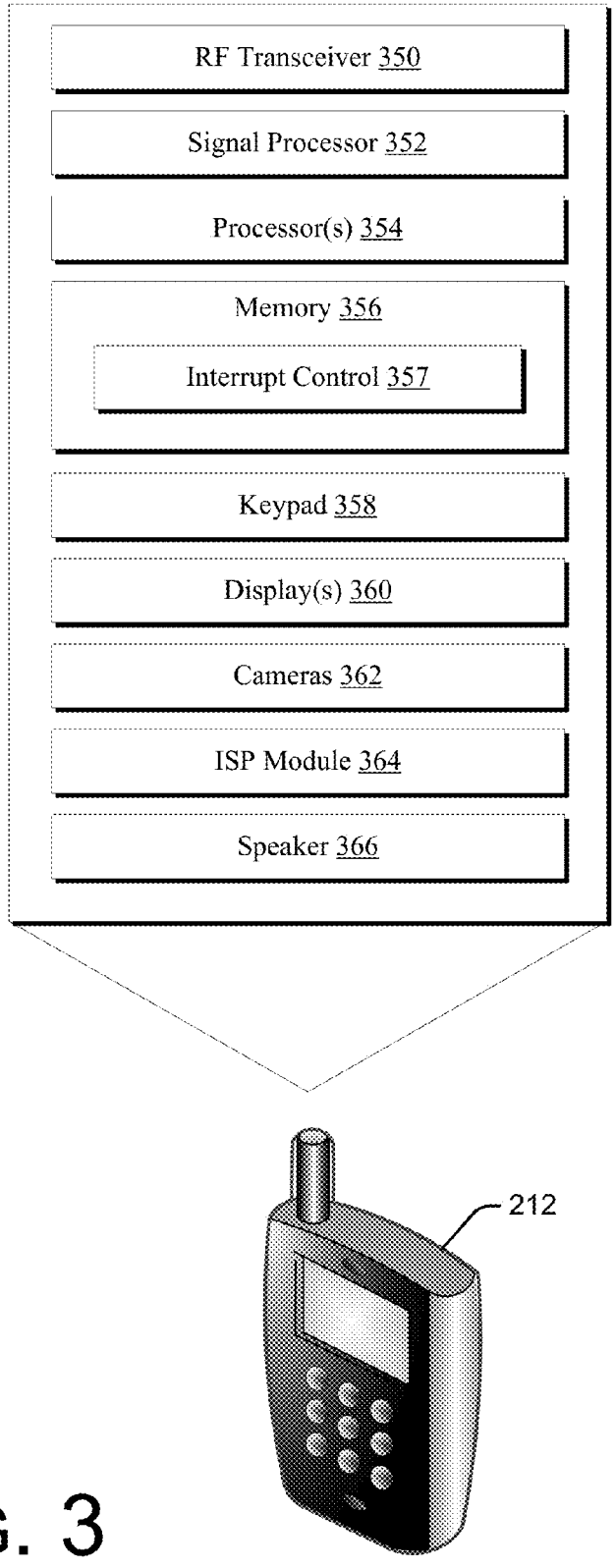
RF Transceiver 350
Signal Processor 352
Processor(s) 354
Memory 356
Interrupt Control 357
Keypad 358
Display(s) 360
Cameras 362
ISP Module 364
Speaker 366
212

FIG. 3

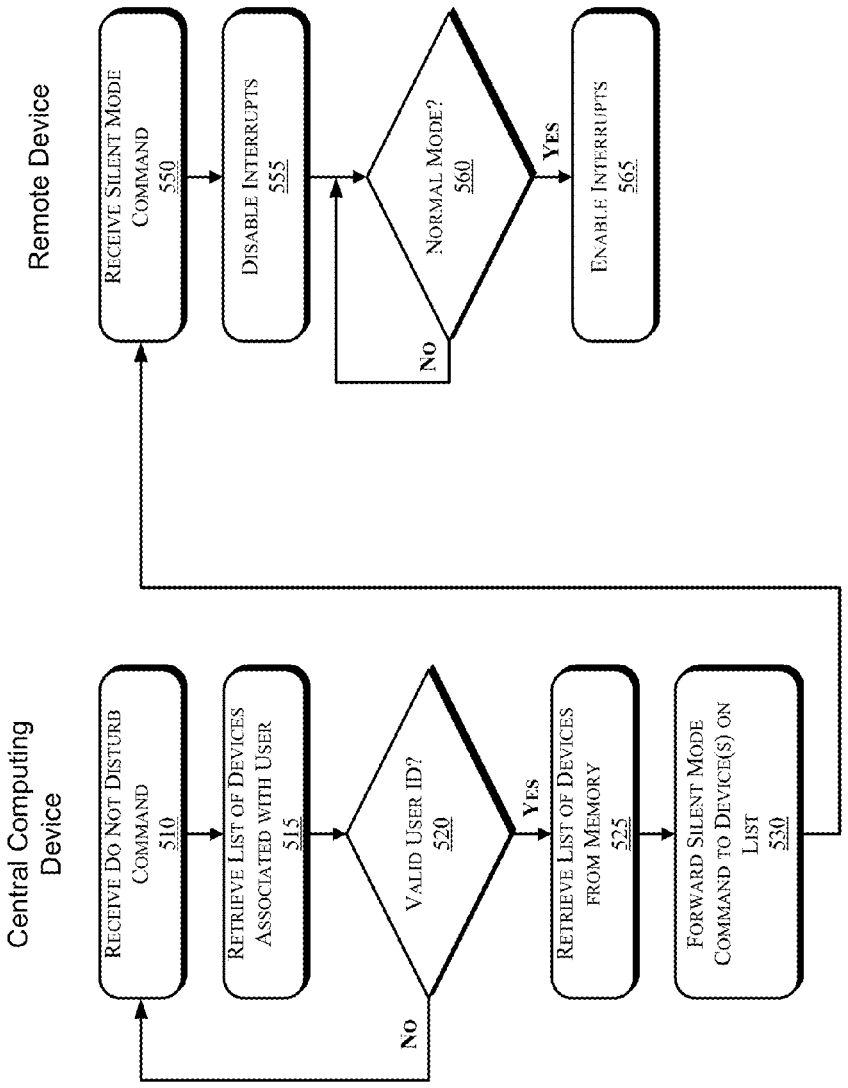
Central Computing Device
Remote Device
Receive Do Not Disturb Command 510
Retrieve List of Devices Associated with User 515
Valid User ID? 520
No
Yes
Retrieve List of Devices from Memory 525
Forward Silent Mode Command to Device(s) on List 530
Receive Silent Mode Command 550
Disable Interrupts 555
Normal Mode? 560
No
Yes
Enable Interrupts 565

FIG. 5

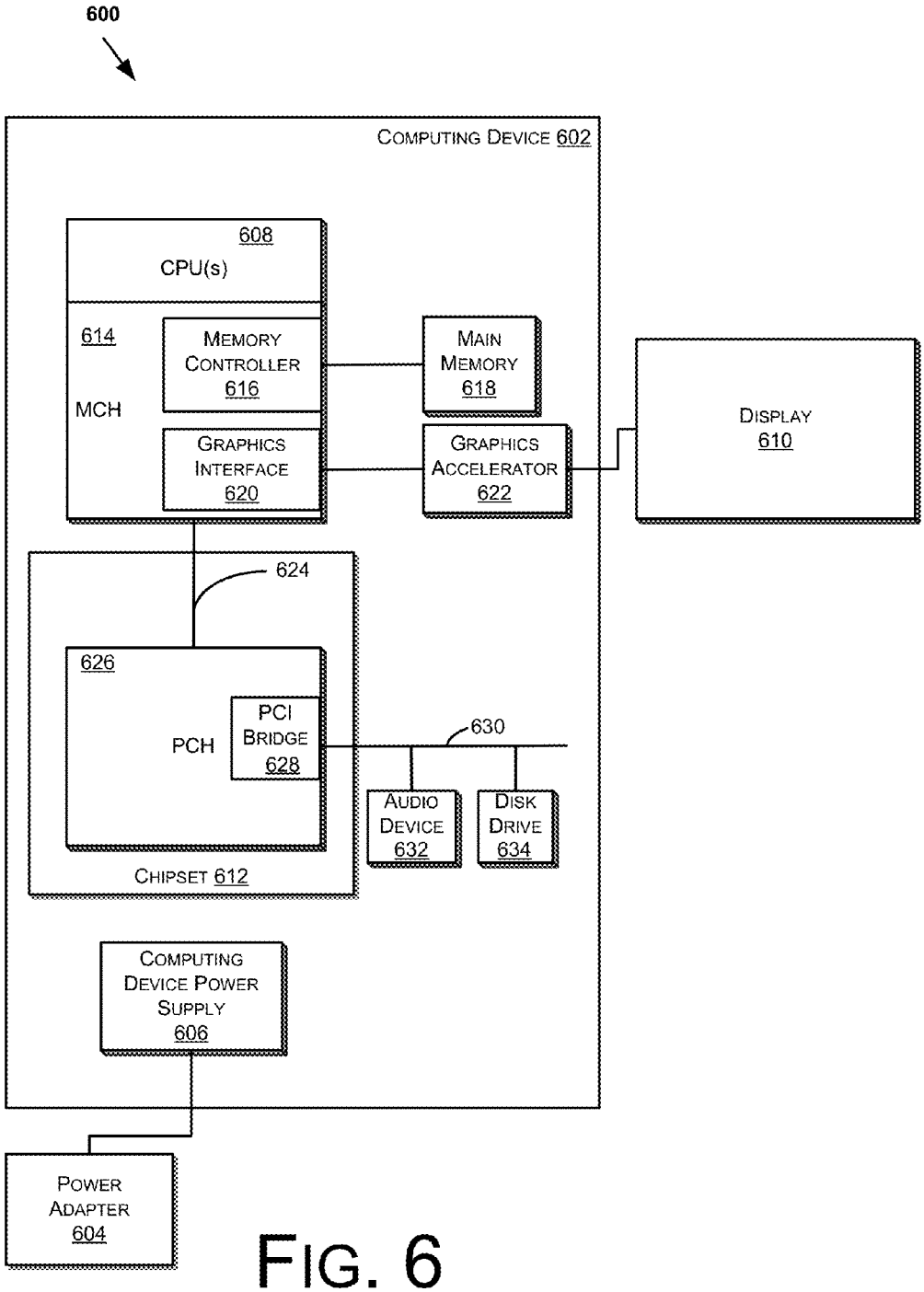
600
COMPUTING DEVICE 602
608
CPU(s)
614
MCH
MEMORY CONTROLLER 616
GRAPHICS INTERFACE 620
MAIN MEMORY 618
GRAPHICS ACCELERATOR 622
DISPLAY 610
624
626
PCH
PCI BRIDGE 628
630
AUDIO DEVICE 632
DISK DRIVE 634
CHIPSET 612
COMPUTING DEVICE POWER SUPPLY 606
POWER ADAPTER 604

FIG. 6

INTERRUPT BLOCKER

RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 12/827,554 filed Jun. 30, 2010, entitled "Interrupt Blocker", now U.S. Pat. No. 8,549,201 issued Oct. 1, 2013.

BACKGROUND

The subject matter described herein relates generally to the field of electronic devices and more particularly to a system and method to block interrupts on one or more electronic devices.

Some electronic devices, or software executing thereon, generate interrupts or notices in response to certain conditions. By way of example, electronic devices such as mobile phones generate an interrupt in response to an incoming call, electronic mail message, or text message. Similarly, personal computers may generate an interrupt in response to an incoming electronic mail message, instant message, or in response to an event on a calendar program. In some contexts these interrupts may be a distraction. Accordingly techniques to block interrupts may find utility.

BRIEF DESCRIPTION OF THE DRAWINGS

The detailed description is described with reference to the accompanying figures.

FIG. **1** is a schematic illustration of an exemplary computing device which may be used to block interrupts in accordance with some embodiments.

FIG. **2** is a schematic illustration of an exemplary networking environment in which a computing device may block interrupts in one or more remote devices in accordance with some embodiments.

FIG. **3** is a schematic illustration of a remote device adapted to to block interrupts in accordance with some embodiments.

FIG. **4** is a flowchart illustrating operations in part of a method to block interrupts, according to embodiments.

FIG. **5** is a flowchart illustrating operations in part of a method to block interrupts, according to embodiments.

FIG. **6** is a schematic illustration of an electronic device which may be adapted to be locked, according to an embodiment.

DETAILED DESCRIPTION

Described herein are exemplary systems and methods to block interrupts in electronic devices. In the following description, numerous specific details are set forth to provide a thorough understanding of various embodiments. However, it will be understood by those skilled in the art that the various embodiments may be practiced without the specific details. In other instances, well-known methods, procedures, components, and circuits have not been illustrated or described in detail so as not to obscure the particular embodiments.

FIG. **1** is a schematic illustration of an exemplary computing device which may be used to block interrupts in accordance with some embodiments. In one embodiment, system **100** includes an electronic device **108** and one or more accompanying input/output devices including a display **102** having a screen **104**, one or more speakers **106**, a keyboard **110**, one or more other I/O device(s) **112**, and a mouse **114**. The other I/O device(s) **112** may include a touch screen, a voice-activated input device, a track ball, and any other device that allows the system **100** to receive input from a user.

In various embodiments, the electronic device **108** may be embodied as a personal computer, a laptop computer, a personal digital assistant, a mobile telephone, an entertainment device, or another computing device. The electronic device **108** includes system hardware **120** and memory **130**, which may be implemented as random access memory and/or read-only memory. A file store **180** may be communicatively coupled to computing device **108**. File store **180** may be internal to computing device **108** such as, e.g., one or more hard drives, CD-ROM drives, DVD-ROM drives, or other types of storage devices. File store **180** may also be external to computer **108** such as, e.g., one or more external hard drives, network attached storage, or a separate storage network.

System hardware **120** may include one or more processors **122**, one or more graphics processors **124**, network interfaces **126**, and bus structures **128**. In one embodiment, processor **122** may be embodied as an Intel® Core2 Duo® processor available from Intel Corporation, Santa Clara, Calif., USA. As used herein, the term "processor" means any type of computational element, such as but not limited to, a microprocessor, a microcontroller, a complex instruction set computing (CISC) microprocessor, a reduced instruction set (RISC) microprocessor, a very long instruction word (VLIW) microprocessor, or any other type of processor or processing circuit.

Graphics processor(s) **124** may function as adjunct processor that manages graphics and/or video operations. Graphics processor(s) **124** may be integrated onto the motherboard of computing system **100** or may be coupled via an expansion slot on the motherboard.

In one embodiment, network interface **126** could be a wired interface such as an Ethernet interface (see, e.g., Institute of Electrical and Electronics Engineers/IEEE 802.3-2002) or a wireless interface such as an IEEE 802.11 compliant interface (see, e.g., IEEE Standard for IT-Telecommunications and information exchange between systems LAN/MAN—Part II: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications Amendment 4: Further Higher Data Rate Extension in the 2.4 GHz Band, 802.11G-2003). Another example of a wireless interface would be a general packet radio service (GPRS) interface (see, e.g., Guidelines on GPRS Handset Requirements, Global System for Mobile Communications/GSM Association, Ver. 3.0.1, December 2002).

Bus structures **128** connect various components of system hardware **128**. In one embodiment, bus structures **128** may be one or more of several types of bus structure(s) including a memory bus, a peripheral bus or external bus, and/or a local bus using any variety of available bus architectures including, but not limited to, 11-bit bus, Industrial Standard Architecture (ISA), Micro-Channel Architecture (MSA), Extended ISA (EISA), Intelligent Drive Electronics (IDE), VESA Local Bus (VLB), Peripheral Component Interconnect (PCI), Universal Serial Bus (USB), Advanced Graphics Port (AGP), Personal Computer Memory Card International Association bus (PCMCIA), and Small Computer Systems Interface (SCSI).

Memory **130** may include an operating system **140** for managing operations of computing device **108**. In one embodiment, operating system **140** includes a hardware interface module **154** that provides an interface to system hardware **120**. In addition, operating system **140** may include a file system **150** that manages files used in the operation of com-

puting device **108** and a process control subsystem **152** that manages processes executing on computing device **108**.

Operating system **140** may include (or manage) one or more communication interfaces that may operate in conjunction with system hardware **120** to transceive data packets and/or data streams from a remote source. Operating system **140** may further include a system call interface module **142** that provides an interface between the operating system **140** and one or more application modules resident in memory **130**. Operating system **140** may be embodied as a UNIX operating system or any derivative thereof (e.g., Linux, Solaris, etc.) or as a Windows® brand operating system, or other operating systems.

In one embodiment, memory **130** includes an interrupt control module **162** which cooperates with one or more remote devices to block interrupts on the one or more remote devices. In one embodiment, the interrupt control module **162** may be may be embodied as logic instructions stored in the computer readable memory module **130** of the system **100**. In various embodiments the interrupt control module **162** may be reduced to firmware which may be stored with a basic input/output system (BIOS) for the system **100**, or to hard-wired logic circuitry, e.g., an integrated circuit (IC). Additional details about the operations implemented by interrupt control module **162** are described below.

FIG. **2** is a schematic illustration of an exemplary networking environment in which a computing device may block interrupts in one or more remote devices in accordance with some embodiments. Networking environment **200** may comprise a one or more computing devices **108***a*, **108***b* (referred to generally by **108**) connected to one or more remote electronic devices **212***a*, **212***b*, **212***c* (referred to generally by **212**) by a one or more communication networks **220**

Computing devices **108** may be implemented as, e.g., a networked computer, a laptop computer, a desktop computer, an electronic device as described with reference to the computing device **108** in FIG. **1**. The communication network(s) **220** may be implemented as a Personal Area Network (PAN), Local Area Network (LAN), Metropolitan Area Network (MAN) or a Wide Area Network (WAN) or the like. Furthermore, communication network **220** may comprise one or more sub-networks. By way of example, and not by limitation, communication network **220** may comprise one or more wireless access points (WAPs) that establish a wireless network, which is coupled to a LAN or directly to a backbone network such as the Internet. Additionally, the communication network **220** may include a variety of input/output transports such as, but not limited to; wired USB or serial links, Wireless 802.11x link, wireless USB, Blue-tooth, infra red link or the like.

One or more of the electronic devices **212** may include a mobile communication/computing device such as a smart phone **212***a*, a pager, **212***b*, or a tablet computing device **212***c*. FIG. **3** is a schematic illustration of an electronic device **212** according to some embodiments. Referring to FIG. **3**, in some embodiments electronic device **212** may be embodied as a mobile telephone, a personal digital assistant (PDA), a laptop computer, or the like. Electronic device **212** may include an RF transceiver **350** to transceive RF signals and a signal processing module **352** to process signals received by RF transceiver **350**.

RF transceiver **350** may implement a local wireless connection via a protocol such as, e.g., Bluetooth or 802.11X. IEEE 802.11a, b or g-compliant interface (see, e.g., IEEE Standard for IT-Telecommunications and information exchange between systems LAN/MAN—Part II: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications Amendment 4: Further Higher Data Rate Extension in the 2.4 GHz Band, 802.11G-2003). Another example of a wireless interface would be a general packet radio service (GPRS) interface (see, e.g., Guidelines on GPRS Handset Requirements, Global System for Mobile Communications/GSM Association, Ver. 3.0.1, December 2002).

Remote device **212** may further include one or more processors **354** and a memory module **356**. As used herein, the term "processor" means any type of computational element, such as but not limited to, a microprocessor, a microcontroller, a complex instruction set computing (CISC) microprocessor, a reduced instruction set (RISC) microprocessor, a very long instruction word (VLIW) microprocessor, or any other type of processor or processing circuit. In some embodiments, processor **354** may be one or more processors in the family of Intel® PXA27x processors available from Intel® Corporation of Santa Clara, Calif. Alternatively, other CPUs may be used, such as Intel's Itanium®, XEON™, ATOM™, and Celeron® processors. Also, one or more processors from other manufactures may be utilized. Moreover, the processors may have a single or multi core design. In some embodiments, memory module **356** includes random access memory (RAM); however, memory module **356** may be implemented using other memory types such as dynamic RAM (DRAM), synchronous DRAM (SDRAM), and the like.

Electronic device **212** may further include one or more input/output interfaces such as, e.g., a keypad **358** and one or more displays **360**, and one or more speakers **366**. In some embodiments electronic device **212** comprises one or more camera modules **362** and an image signal processor **364**.

In some embodiments electronic device **212** may include an interrupt control module **357**. Interrupt control module **357** cooperates with the interrupt control module **162** in computing device **108** to block interrupts on electronic device in a programmatic fashion. By way of example, in some embodiments a list of electronic devices associated with a user may be stored in the memory of computing device **108**. The list may include the computing device **108** and one or more electronic devices **212**. A do not disturb command may be entered in the computing device, which triggers the computing device **108** to send a silent mode command to one or more electronic devices **212** associated with the user. The electronic device(s) **212** may block interrupts generated by the operation of the device(s) **212**.

Operations for blocking interrupts are described with reference to FIG. **4** and FIG. **5**. In some embodiments the operations of FIG. **4** may be implemented by the interrupt control module **162** on computing device **108**. The operations of FIG. **5** may be implemented by the interrupt control module **162** on computing device **108** and the interrupt control module **357** on the electronic device(s) **212**.

Referring first to FIG. **4**, in some embodiments a user identifier (ID) may be associated with one or more computing devices **108** and one or more electronic devices **212**. Thus, at operation **410** a user ID is received, and at operation **415** one or more electronic device IDs are received. In some embodiments a user may enter a user ID and device IDs into the computing device **108** via a keyboard **110** or another input/output device.

At operation **420** a logical relationship is established between the user ID and the one or more electronic device IDs. By way of example, the user ID and the device ID may be stored in record. At operation **425** the record is stored in a memory module **130** coupled to computing device **108**, e.g., the memory module **130** or the file store **180**.

In some embodiments the computing device **108** may maintain additional information associated with the electronic device(s) **212** associated with a user. By way of example, the computing device **108** may maintain a network address and an operational status for one or more electronic devices **212**. In another embodiment the computing device **108** may maintain location information associated with the electronic device(s) **212** associated with a user.

Referring now to FIG. **5**, at operation **510** a do not disturb command may be entered in the computing device **108**. By way of example a use may enter a do not disturb command directly into computing device **108** via a keyboard or other input/output device. Alternatively, a user may enter a do not disturb command via a remote device, including one or more of the electronic devices **212** coupled to computing device **108**. Alternatively, a do not disturb command may be entered by a software module executing on computing device **108** or a remote device. By way of example, a calendar program may be configured to schedule a do not disturb command for a particular time and day. In some embodiments the do not disturb command includes a user ID.

If, at operation **515**, the user ID is not valid, then control passes back to operation **510** and a new ID may be entered. By contrast, if at operation **515** the user ID is valid, then control passes to operation **520** and the record associated with the user ID is retrieved from memory **130** or file store **180** (operation **525**). At operation **530** a silent mode command is forwarded to one or more devices on the list of electronic devices **212** associated with the user ID. In some embodiments all electronic devices **212** associated with the user ID may be notified, while in other embodiments only a subset of devices may be notified.

At operation **550** the silent mode command is received in the one or more electronic device(s) **212** associated with the user ID. At operation **555** the interrupt control module **357** on the electronic device(s) **212** disables interrupts on the device (s) **212**. By way of example, in some embodiments the interrupt control module **357** may override the operations of one or more applications executing on the device(s) **212** to block any alerts issued by the application(s). In other embodiments the interrupt control module **357** may operate at the hardware level, e.g., by blocking the output of a speaker on the electronic device(s) **212**.

At operation **560** it is determined whether the device(s) **212** should be restored to a normal operating mode. By way of example, the interrupt control module **357** may return the electronic device **212** to a normal operating mode in response to a normal mode command from the computing device **108**, or after a predetermined amount of time has elapsed. If, at operation **560** no events have occurred to return the electronic device(s) back to a normal operating mode, then the electronic device(s) **212** continue operating in silent mode and wait for an event to return to normal operating mode. By contrast, if at operation **560** an event has occurred to return the electronic device(s) **212** then control passes to operation **565** and the electronic device(s) are returned to normal operating mode in which interrupts are allowed.

As described above, in some embodiments the electronic device **108** may be embodied as a computer system. FIG. **6** is a schematic illustration of a computer system **600** in accordance with some embodiments. The computer system **600** includes a computing device **602** and a power adapter **604** (e.g., to supply electrical power to the computing device **602**). The computing device **602** may be any suitable computing device such as a laptop (or notebook) computer, a personal digital assistant, a desktop computing device (e.g., a workstation or a desktop computer), a rack-mounted computing device, and the like.

Electrical power may be provided to various components of the computing device **602** (e.g., through a computing device power supply **606**) from one or more of the following sources: one or more battery packs, an alternating current (AC) outlet (e.g., through a transformer and/or adaptor such as a power adapter **604**), automotive power supplies, airplane power supplies, and the like. In some embodiments, the power adapter **604** may transform the power supply source output (e.g., the AC outlet voltage of about 110VAC to 240VAC) to a direct current (DC) voltage ranging between about 5VDC to 12.6VDC. Accordingly, the power adapter **604** may be an AC/DC adapter.

The computing device **602** may also include one or more central processing unit(s) (CPUs) **608**. In some embodiments, the CPU **608** may be one or more processors in the Pentium® family of processors including the Pentium® II processor family, Pentium® III processors, Pentium® IV, or CORE2 Duo processors available from Intel® Corporation of Santa Clara, Calif. Alternatively, other CPUs may be used, such as Intel's Itanium®, XEON™, and Celeron® processors. Also, one or more processors from other manufactures may be utilized. Moreover, the processors may have a single or multi core design.

A chipset **612** may be coupled to, or integrated with, CPU **608**. The chipset **612** may include a memory control hub (MCH) **614**. The MCH **614** may include a memory controller **616** that is coupled to a main system memory **618**. The main system memory **618** stores data and sequences of instructions that are executed by the CPU **608**, or any other device included in the system **600**. In some embodiments, the main system memory **618** includes random access memory (RAM); however, the main system memory **618** may be implemented using other memory types such as dynamic RAM (DRAM), synchronous DRAM (SDRAM), and the like. Additional devices may also be coupled to the bus **610**, such as multiple CPUs and/or multiple system memories.

The MCH **614** may also include a graphics interface **620** coupled to a graphics accelerator **622**. In some embodiments, the graphics interface **620** is coupled to the graphics accelerator **622** via an accelerated graphics port (AGP). In some embodiments, a display (such as a flat panel display) **640** may be coupled to the graphics interface **620** through, for example, a signal converter that translates a digital representation of an image stored in a storage device such as video memory or system memory into display signals that are interpreted and displayed by the display. The display **640** signals produced by the display device may pass through various control devices before being interpreted by and subsequently displayed on the display.

A hub interface **624** couples the MCH **614** to an platform control hub (PCH) **626**. The PCH **626** provides an interface to input/output (I/O) devices coupled to the computer system **600**. The PCH **626** may be coupled to a peripheral component interconnect (PCI) bus. Hence, the PCH **626** includes a PCI bridge **628** that provides an interface to a PCI bus **630**. The PCI bridge **628** provides a data path between the CPU **608** and peripheral devices. Additionally, other types of I/O interconnect topologies may be utilized such as the PCI Express™ architecture, available through Intel® Corporation of Santa Clara, Calif.

The PCI bus **630** may be coupled to an audio device **632** and one or more disk drive(s) **634**. Other devices may be coupled to the PCI bus **630**. In addition, the CPU **608** and the MCH **614** may be combined to form a single chip. Further-

more, the graphics accelerator **622** may be included within the MCH **614** in other embodiments.

Additionally, other peripherals coupled to the PCH **626** may include, in various embodiments, integrated drive electronics (IDE) or small computer system interface (SCSI) hard drive(s), universal serial bus (USB) port(s), a keyboard, a mouse, parallel port(s), serial port(s), floppy disk drive(s), digital output support (e.g., digital video interface (DVI)), and the like. Hence, the computing device **602** may include volatile and/or nonvolatile memory.

The terms "logic instructions" as referred to herein relates to expressions which may be understood by one or more machines for performing one or more logical operations. For example, logic instructions may comprise instructions which are interpretable by a processor compiler for executing one or more operations on one or more data objects. However, this is merely an example of machine-readable instructions and embodiments are not limited in this respect.

The terms "computer readable medium" as referred to herein relates to media capable of maintaining expressions which are perceivable by one or more machines. For example, a computer readable medium may comprise one or more storage devices for storing computer readable instructions or data. Such storage devices may comprise storage media such as, for example, optical, magnetic or semiconductor storage media. However, this is merely an example of a computer readable medium and embodiments are not limited in this respect.

The term "logic" as referred to herein relates to structure for performing one or more logical operations. For example, logic may comprise circuitry which provides one or more output signals based upon one or more input signals. Such circuitry may comprise a finite state machine which receives a digital input and provides a digital output, or circuitry which provides one or more analog output signals in response to one or more analog input signals. Such circuitry may be provided in an application specific integrated circuit (ASIC) or field programmable gate array (FPGA). Also, logic may comprise machine-readable instructions stored in a memory in combination with processing circuitry to execute such machine-readable instructions. However, these are merely examples of structures which may provide logic and embodiments are not limited in this respect.

Some of the methods described herein may be embodied as logic instructions on a computer-readable medium. When executed on a processor, the logic instructions cause a processor to be programmed as a special-purpose machine that implements the described methods. The processor, when configured by the logic instructions to execute the methods described herein, constitutes structure for performing the described methods. Alternatively, the methods described herein may be reduced to logic on, e.g., a field programmable gate array (FPGA), an application specific integrated circuit (ASIC) or the like.

In the description and claims, the terms coupled and connected, along with their derivatives, may be used. In particular embodiments, connected may be used to indicate that two or more elements are in direct physical or electrical contact with each other. Coupled may mean that two or more elements are in direct physical or electrical contact. However, coupled may also mean that two or more elements may not be in direct contact with each other, but yet may still cooperate or interact with each other.

Reference in the specification to "one embodiment" or "some embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least an implementation. The appearances of the phrase "in one embodiment" in various places in the specification may or may not be all referring to the same embodiment.

Although embodiments have been described in language specific to structural features and/or methodological acts, it is to be understood that claimed subject matter may not be limited to the specific features or acts described. Rather, the specific features and acts are disclosed as sample forms of implementing the claimed subject matter.

What is claimed is:

1. An apparatus, comprising:
logic to:
associate a plurality of communication devices with a user;
determine the user has a do not disturb status at a first time; and
forward a silent mode command to at least one communication device of the plurality of communication devices associated with the user, wherein the silent mode command causes the at least one communication device to block incoming alerts generated by one or more applications executing on the at least one communication device.

2. The apparatus of claim **1**, comprising logic to:
determine the user does not have the do not disturb status at a second time; and
allow incoming communications from one or more of the plurality of communication devices at the second time in response to the lack of the do not disturb status.

3. The apparatus of claim **1**, wherein the silent mode command causes the at least one communication device to block an output of a speaker on the at least one communication device.

4. The apparatus of claim **1**, wherein the incoming communications comprises one or more of an email, a text message, and a phone call.

5. The apparatus of claim **1**, wherein the do not disturb status determination comprises referencing calendar data associated with the user.

6. The apparatus of claim **1**, wherein the do not disturb status determination comprises receiving a do not disturb status from the user.

7. A non-transitory machine-readable medium to store instructions, the instructions, when read by a machine, to cause the machine to:
associate a plurality of communication devices with a user;
determine the user has a do not disturb status at a first time; and
forward a silent mode command to at least one communication device of the plurality of communication devices associated with the user, wherein the silent mode command causes the at least one communication device to block incoming alerts generated by one or more applications executing on the at least one communication device.

8. The non-transitory machine-readable medium of claim **7**, wherein the non-transitory machine readable medium comprises instructions to further cause the machine to:
determine the user does not have the do not disturb status at a second time;
and
allow incoming communications from one or more of the plurality of communication devices at the second time in response to the lack of the do not disturb status.

9. The non-transitory machine-readable medium of claim **7**, wherein the silent mode command causes the at least one

communication device to block an output of a speaker on the at least one communication device.

10. The non-transitory machine-readable medium of claim **7**, wherein the incoming communications comprises one or more of an email, a text message, and a phone call.

11. The non-transitory machine-readable medium of claim **7**, wherein the do not disturb status determination comprises referencing calendar data associated with the user.

12. The non-transitory machine-readable medium of claim **7**, wherein the do not disturb status determination comprises receiving a do not disturb status from the user.

13. An electronic device, comprising:

at least one processor; and

logic to:

associate a plurality of communication devices with a user;

determine the user has a do not disturb status at a first time; and

forward a silent mode command to at least one communication device of the plurality of communication devices associated with the user, wherein the silent mode command causes the at least one communication device to block incoming alerts generated by one or more applications executing on the at least one communication device.

14. The electronic device of claim **13**, comprising logic to:

determine the user does not have the do not disturb status at a second time; and

allow incoming communications from one or more of the plurality of communication devices at the second time in response to the lack of the do not disturb status.

15. The electronic device of claim **13**, wherein the silent mode command causes the at least one communication device to block an output of a speaker on the at least one communication device.

16. The electronic device of claim **13**, wherein the incoming communications comprises one or more of an email, a text message, and a phone call.

17. The electronic device of claim **13**, wherein the do not disturb status determination comprises referencing calendar data associated with the user.

18. The electronic device of claim **13**, wherein the do not disturb status determination comprises receiving a do not disturb status from the user.

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